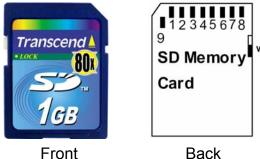
# TS128M~1GSD80

## 80x Secure Digital Card

#### Description

Secure Digital Card is a compact, slim and high capacity storage media with copyright protection. Designed in advanced SD specification Ver.1.1, Transcend 80x SD card now reaches a new performance milestone. Based on 0.18um process controller and high quality SLC (Single-Level-Cell) NAND Flash chip, Transcend 80x SD card can provide high performance, low power consumption yet excellent reliability.

#### Placement



## Front

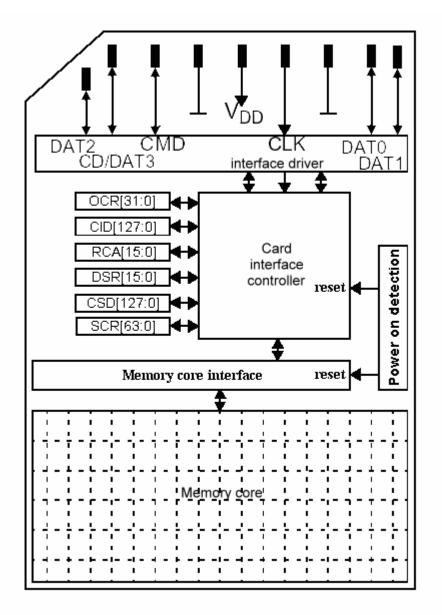
#### **Pin Definition**

#### Features

- · ROHS compliant product
- Operating Voltage: 2.7 ~ 3.6V
- Operating Temperature: -25 ~ 85°C
- Insertion/removal durability: 10,000 cycles
- Fully compatible with SD card spec. v1.1
- Support SD command class 0,2,4,5,6,7,8
- Mechanical Write Protection Switch
- Forward compatibility to MultiMediaCard Version 2.11
- Supports Copy Protection for Recorded Media(CPRM) for music and other commercial media
- Form Factor: 24mm x 32mm x 2.1mm

Din Ma			SD Mode			SPI Mode
Pin No.	Pin No. Name Type Description		Description	Name	Туре	Description
1	CD/DAT3	I/O/PP	Card Detect/Data Line [Bit3]	CS	Ι	Chip Select (neg true)
2	CMD	PP	Command/Response	DI	Ι	Data In
3	V <sub>SS1</sub>	S	Supply voltage ground	VSS	S	Supply voltage ground
4	V <sub>DD</sub>	S	Supply voltage	VDD	S	Supply voltage
5	CLK	I	Clock	SCLK	Ι	Clock
6	V <sub>SS2</sub>	S	Supply voltage ground	VSS2	S	Supply voltage ground
7	DAT0	I/O/PP	Data Line [Bit0]	DO	O/PP	Data Out
8	DAT1	I/O/PP	Data Line [Bit1]	RSV		
9	DAT2	I/O/PP	Data Line [Bit2]	RSV		

## Architecture



## **Bus Operating Conditions**

#### General

Parameter	Symbol	Min.	Max.	Unit	Remark	
Peak voltage on all lines		-0.3	VDD+0.3	V		
All Inputs						
Input Leakage Current		-10	10	μA		
All Outputs						
Output Leakage Current		-10	10	μA		

#### • Power Supply Voltage

Parameter	Symbol	Min.	Max.	Unit	Remark
Supply voltage	$V_{DD}$	2.0	3.6	V	CMD0, 15,55,ACMD41
					commands
Supply voltage specified in OCR register		2.7	3.6	V	Except CMD0, 15,55,
					ACMD41 commands
Supply voltage differentials ( $V_{SS1}$ , $V_{SS2}$ )		-0.3	0.3	V	
Power up time			250	ms	From 0v to V <sub>DD</sub> Min.

#### Bus Signal Line Load

The total capacitance  $C_L$  the CLK line of the SD Memory Card bus is the sum of the bus master capacitance  $C_{HOST}$ , the bus capacitance  $C_{BUS}$  itself and the capacitance  $C_{CARD}$  of each card connected to this line:  $C_L = C_{HOST} + C_{BUS} + N^*C_{CARD}$ 

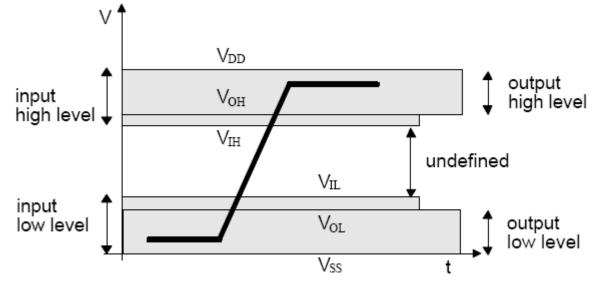
Parameter	Symbol	Min.	Max.	Unit	Remark
Bus signal line capacitance	CL		100	pF	$f_{PP} \le 20$ MHz, 7 cards
Single card capacitance			10	pF	
Maximum signal line inductance			16	nH	f <sub>PP</sub> ≤ 20 MHz
Pull-up resistance inside card (pin1)	R <sub>DAT3</sub>	10	90	kΩ	May be used for card
					detection

Note that the total capacitance of CMD and DAT lines will be consist of  $C_{HOST}$ ,  $C_{BUS}$  and one  $C_{CARD}$  only since they are connected separately to the SD Memory Card host.

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	$R_{CMD}, R_{DAT}$	10	100	kΩ	To prevent bus floating
Bus signal line capacitance	CL		250	pF	$f_{PP} \le 5 \text{ MHz}$ , 21 cards

## Bus Signal Levels

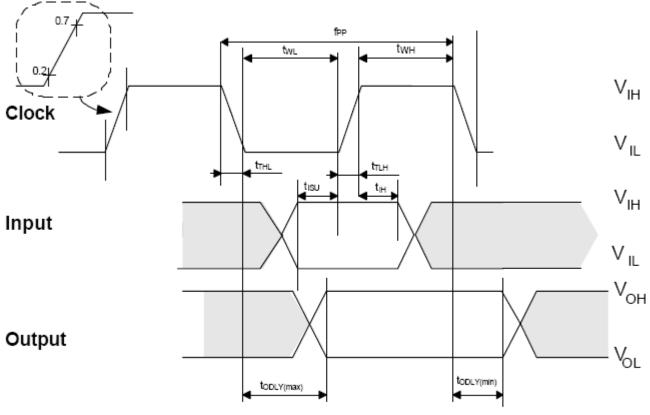
As the bus can be supplied with a variable supply voltage, all signal levels are related to the supply voltage.



To meet the requirements of the JEDEC specification JESD8-1A, the card input and output voltages shall be within the following specified ranges for any  $V_{DD}$  of the allowed voltage range:

Parameter	Symbol	Min.	Max.	Unit	Remark
Output HIGH voltage	V <sub>OH</sub>	0.75* V <sub>DD</sub>		V	I <sub>OH</sub> = -100 μA @V <sub>DD</sub> min
Output LOW voltage	V <sub>OL</sub>		0.125* V <sub>DD</sub>	V	I <sub>OL</sub> = -100 μA @V <sub>DD</sub> min
Input HIGH voltage	V <sub>IH</sub>	0.625* V <sub>DD</sub>	V <sub>DD</sub> + 0.3	V	
Input LOW voltage	V <sub>IL</sub>	$V_{SS} - 0.3$	$0.25*V_{DD}$	V	

## • Bus Timing (Default)



Shaded areas are not valid

## Figure 47: Timing diagram data input/output referenced to clock (Default)

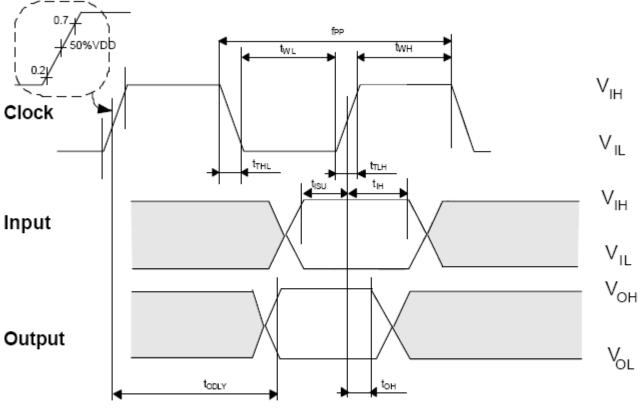
Parameter	Symbol	Min	Max.	Unit	Remark	
Clock CLK (All values are referred to min ( $V_{IH}$ ) a	Clock CLK (All values are referred to min (V <sub>IH</sub> ) and max (V <sub>IL</sub> )					
Clock frequency Data Transfer Mode	f <sub>PP</sub>	0	25	MHz	$C_L \le 100 \text{ pF}$ , (7 cards)	
Clock frequency Identification Mode	f <sub>OD</sub>	0	400	KHz	$C_L \le 250 \text{ pF}$ , (21 cards)	
(The low freq. is required for MultiMediaCard						
compatibility.)						
Clock low time	t <sub>vvL</sub>	10		ns	$C_L \leq 100 \text{ pF}$ , (7 cards)	
		50		ns	$C_L \le 250 \text{ pF}$ , (21 cards)	
Clock high time	t <sub>WH</sub>	10		ns	$C_L \le 100 \text{ pF}$ , (7 cards)	
		50		ns	$C_L \le 250 \text{ pF}$ , (21 cards)	
Clock rise time	$t_{TLH}$		10	ns	$C_L \le 100 \text{ pF}$ , (7 cards)	

# TS128M~1GSD80

# 80x Secure Digital Card

			50	ns	$C_L \le 250 \text{ pF}$ , (21 cards)	
Clock fall time	t <sub>THL</sub>		10	ns	$C_L \leq 100 \text{ pF}$ , (7 cards)	
			50	ns	$C_L \le 250 \text{ pF}$ , (21 cards)	
Inputs CMD, DAT (referenced to CLK)	Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t <sub>ISU</sub>	5		ns	$C_L \le 25 \text{ pF}, (1 \text{ cards})$	
Input hold time	t <sub>IH</sub>	5		ns	$C_L \le 25 \text{ pF}, (1 \text{ cards})$	
Outputs CMD, DAT (referenced to CLK)						
Output Delay time during Data Transfer Mode	t <sub>ODLY</sub>	0	14	ns	$C_L \le 25 \text{ pF}, (1 \text{ cards})$	
Output Delay time during Identification Mode	t <sub>ODLY</sub>	0	50	ns	$C_{L} \leq 25 \text{ pF}, (1 \text{ cards})$	

### • Bus Timing (High Speed Mode)



Shaded areas are not valid

### Figure 48: Timing diagram data input/output referenced to clock (High-Speed)

Parameter	Symbol	Min	Max.	Unit	Remark		
Clock CLK (All values are referred to min (VIH) a	Clock CLK (All values are referred to min ( $V_{H}$ ) and max ( $V_{L}$ )						
Clock frequency Data Transfer Mode	f <sub>PP</sub>	0	50	MHz			
Clock low time	t <sub>WL</sub>	7		ns			
Clock high time	t <sub>WH</sub>	7		ns			
Clock rise time	t <sub>TLH</sub>		3	ns			
Clock fall time	t <sub>THL</sub>		3	ns			
Inputs CMD, DAT (referenced to CLK)	Inputs CMD, DAT (referenced to CLK)						
Input set-up time	t <sub>ISU</sub>	6		ns			
Input hold time	t <sub>IH</sub>	2		ns			
Outputs CMD, DAT (referenced to CLK)							

# TS128M~1GSD80

Output Delay time during Data Transfer Mode	t <sub>ODLY</sub>		14	ns	
Output Hold time	t <sub>он</sub>	2.5		ns	
Total System capacitance for each line	CL		40	pF	

## Reliability and Durability

Temperature	Operation: -25°C / 85°C (Target spec)
Moisture and corrosion	Operation: 25°C / 95% rel. humidity
	Storage: 40°C / 93% rel. hum./500h
	Salt Water Spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10.000 mating cycles
Bending	10N
Torque	0.15N.m or +/-2.5 deg
Drop test	1.5m free fall
UV light exposure	UV: 254nm, 15Ws/cm <sup>2</sup> according to ISO 7816-1
Visual inspection	No warpage; no mold skin; complete form; no cavities surface smoothness <= -0.1
Shape and form	mm/cm <sup>2</sup> within contour; no cracks; no pollution (fat, oil dust, etc.)
Minimum moving force of WP witch	40gf (Ensures that the WP switch will not slide while it is inserted to the connector.)
WP Switch cycles	minimum 1000 Cycles(@Slide force 0.4N to 5N)

Above technical information is based on industry standard data and tested to be reliable. However, Transcend makes no warranty, either expressed or implied, as to its accuracy and assumes no liability in connection with the use of this product. Transcend reserves the right to make changes in specifications at any time without prior notice.